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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/895,278	06/29/2001	Mark Anders	10559-403001 / P10340	7194

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EXAMINER

FARAHANI, DANA

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 09/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/895,278

Applicant(s)

ANDERS ET AL. *jk*

Examiner

Dana Farahani

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 July 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al., hereinafter Wada (U.S. 6,225,846) in view of Fujita et al., hereinafter Fujita (U.S. 6,215,159), all previously cited.

Regarding claim 1, Wada discloses in figure 1 an input gate L6 including an input transistor P3 having an input node and an output node. Wada does not disclose two or more clocked input gates operative to place a pre-charge mode in response to a first clock signal and to place the repeater in an evaluate mode in response to a second clock signal. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use clock signals to the gates, since it was known in the art that clock signals are used to operate MOS transistors (see, for example, Fujita, figure 5A).

Regarding claim 2, Wada discloses in figure 1 the transistors include a PMOS transistor P3 coupled to E3 and an NMOS transistor N4 coupled to Vss, the input transistor N3 being connected between said PMOS and NMOS transistors.

3. Claims 3-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada in view of Fujita as applied to claim 1 above, and further in view of Rossi et al., hereinafter Rossi (U.S. 6,069,513).

Regarding claims 3 and 4, Wada discloses in figure 1 an intermediate node coupled to one of a source and a drain of the input transistor N3; an output inverter 2 having an output coupled to the output node and an input coupled to the intermediate node; Wada does not disclose a first transistor having a gate coupled to the input node and one of a source and a drain connected to the intermediate node; and a second transistor connected in series with the first transistor, said second transistor having one of a source and a drain connected to a voltage supply. Rossi discloses in figure 6 a first transistor M4 having a gate coupled to the input node T and one of a source and a drain connected to an intermediate node B; and a second transistor M3 connected in series with the first transistor, said second transistor having one of a source and a drain connected to a voltage supply vdd. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include these transistors in Wada's invention in order to be able to have a pull up transistor at the intermediate node.

Regarding claims 5-10, Wada discloses a feedback inverter 2 where the input of the inverter connected to the intermediate node and an output coupled to a gate of the second transistor P3.

Regarding claims 11-17, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the dynamic repeater in a dynamic bus in order to make the connection between the drivers and the flip flops.

Response to Arguments

4. Applicant's arguments filed on 7/10/02 have been fully considered but they are not persuasive.

Applicant's argument that circuit transistor P3, circuit 4 of figure 1 of Wada reference, can not be considered as an input transistor is not persuasive because transistor P3 receives an input signal from inverter 1. An inverter merely complements the input signal fed to it. Therefore, the signal output from the inverter can be considered an input signal also, so transistor P3 can be considered as an input transistor.

Applicant's allegation that the proper operation of the circuitry in figure 1 of Wada reference "requires that transistors P4 and N4 are always on...Clocking the input gates to these transistors would make the circuit unstable for its intended purpose" is not true. Clocks are provided to the gates of transistors, in general, not necessarily are for the purpose of turning the transistors on and off, but could also be used to control the operation of the circuitry in which the transistor is used by supplying different voltages to the transistors in equal time intervals.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within


TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (703)305-1914. The examiner can normally be reached on M-F 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703)306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Dana Farahani
August 24, 2002


OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800